IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Charles Carpenter

Serial No. **09/864,918**

Filing Date: **05/24/2001**

For: **A METHOF FOR ARRAY PROCESSING OF SURFACE ACOUSTIC WAVE DEVICES**

Examiner: **Paul D. Kim**

Group Art Unit: **3729**

Attorney Docket No. **7631.89**

Asst. Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

DECLARATION OF JACK R. CHOCOLA UNDER 37 CFR § 1.132

I, Jack R. Chocola, do hereby declare and say as follows:

1. I am currently Director of Process Engineering for Sawtek, Inc., assignee for the application identified above. I am very much aware of the surface acoustic wave (SAW) device array processing that is the subject of the patent application. I have a BSEE from the University of Florida at Gainesville, Florida, and a BA in Psychology from Emory University in Atlanta Georgia. I am a citizen of the United States of America and a resident of the State of Florida residing at 171 E. Goodheart Ave., Lake Mary, FL 32746.

2. I joined Sawtek, Inc. in 1995 as the Fabrication Process Engineering Manager. My responsibilities included building a front-end process engineering organization capable of developing and supporting systems and processes needed for volume production of high performance surface acoustic wave devices. In 2001, I was promoted to Director of Process Engineering and assumed responsibility for all front-end and back-end process development and sustaining engineering activities. Prior to coming to Sawtek Inc., I was a Member of the Professional Staff at Lockheed Martin Corporation in Orlando Florida. At Lockheed Martin, I developed processes needed for fabrication and assembly of MESFET and MODFET GaAs devices used in Ka-band and W-band transceiver modules. Before Joining Lockheed Martin in 1985, I was a process engineer at Texas Instruments in Dallas Texas, participating in the development and production of III-V and II-VI compound semiconductor devices.

3. I have been provided with copies of cited patent references including United States Patent Nos. 6, 428, 650 to Chung; 6,321,444 to Yatsuda et al.; 5,824,177 to Yoshimoto et al.; and 5,611,129 to Yoshimoto et al.; as well as the Office Action of 06/25/2004 including the Examiner's remarks for the above referenced application.

4. I have carefully studied these referenced patents with respect to the subject matter of Claims 1, 2, 6, 7, 11-13, 15, 19, and 20 now pending in the application. In this regard, I believe the following information about array processing of SAW devices will be helpful in understanding distinguishing features of the claimed invention.

5. It is my understanding that Yatsuda '444 teaches a process of making a flip-chip SAW device including the steps of forming a material having a first and second surface and a cavity with a recess to receive a lid, and sealing the lid in the recess over the inserted SAW die. Chung '650 teaches an assembly process for a plurality of optical devices and separating a wafer into individual optical devices. The Examiner rejects claims 1,6,7,12,13,15,19 and 20 contending that it would be obvious at the time of invention for a person having ordinary skill in the art to modify the process of fabricating a SAW device of Yatsuda '444 along with the teaching of Chung '650 for fabricating a plurality of optical devices to arrive at the teaching of the claimed invention.

6. As one skilled in the art, I must disagree with the Examiner in this view. In support of my opinion, consider that Yatsuda '444 does not teach array processing of SAW flip-chip devices which comprise the steps of having a plurality of cavities extending into the array from the first surface, inserting a SAW die in a face down arrangement into the plurality of cavities, the plurality of cavities each have a recess for the purpose of receiving a lid, solder sealing the array and separating the array into individual SAW devices. Yatsuda '444 teaches only the assembly of a single SAW flip-chip device with a window to adjust the characteristics of the SAW device. Yatsuda '444 does not teach nor even infer the array processing of the SAW flip-chip packages as claimed.

7. Further consider that Chung '650 teaches an assembly process for a plurality of optical devices including the step of sealing a lid over each inserted optical device using an adhesive preform or a thin layer of electrically conductive material. Using an adhesive preform or a thin layer of electrically conductive material over each optical devices results in a non-hermetically sealed structure. While the sealing of devices using adhesive preforms, molded epoxy, polymer or plastic as taught by Chung (col.5 lines 10-13) may provide resistance to the passage of liquid water into the device but will not prevent water vapor from entering the package. Such processes are not considered as "hermetically sealing" by those skilled in the art. SAW devices are not typically passivated so the presence of water vapor inside the package could result in damage to the unprotected device. Similarly, the sealing of a metal lid with a thin layer of electrically conductive material, as taught by Chung '650 (col. 5 lines 31- 47) would provide electrostatic and/or electromagnetic shielding and resistance to the passage of liquid water to within the package but will not prevent water vapor from entering the package. To one of skill in the art, it is not considered as hermetically sealing. Specifically, Chung '650 is not directed to nor does it suggest the assembly process of an array of hermetically sealed small dimension flip-chip SAW devices. One of skill in the art relying on Chung '650 would not be aware of the challenging task of accomplishing a technique of externally fixturing the soldered lids onto an array of very

small dimensioned cavities holding the flip-chip SAW die. The small dimensions of the lids associated with flip-chip SAW devices and the limited clearance between packages on the array make it difficult to maintain integrity between the external fixture and the array during solder reflow. The problem of solder bridging between the lids is prevalent. Further, it would appear that Chung '650 teaches away from solder sealing to achieve hermetically sealed device stating that true hermetically sealed packages are very expensive to fabricate (col. 1 lines 65 – 67). The claimed invention provides the teaching of forming a recess in the cavity such that the walls of the recess contain the lids during handling and prevent solder from bridging between the lids during solder reflow of the array. Neither Yatsuda '444 nor Chung '650 suggest or infer this teaching. One skilled in the art would not find the claimed invention obvious based on the teachings of Yatsuda '444 and Chung '650.

8. The Examiner rejects Claims 2 and 11 as being unpatentable over Yoshimoto '129 in view of Chung '650 and further in view of Yoshihara '177. Yoshimoto '129 teaches a method of assembling bulk wave piezoelectric oscillators in an array of resinous packages. Since the package is resinous, it is well known to those of skill in the art that it would not provide a hermetic seal. Yoshimoto '129 teaches assembly of bulk wave devices and not surface acoustic wave devices mounted in a flip-chip arrangement in an array. As above discussed, Chung '650 teaches an assembly process of optical devices, which includes the step of sealing the optical devices using adhesive preforms or a thin layer of electrically conductive layer, which results in a non-hermetically sealed device. Neither Chung '650 nor Yoshimoto '129 teach a method of manufacturing an array of hermetically sealed surface acoustic wave devices, with the method comprising the steps of forming a recess within the cavity of the array, inserting and attaching a SAW die face down (in a flip-chip arrangement), and solder sealing a metal lid in the recess over the inserted SAW die to hermetically seal the SAW die within the cavity. To one skilled in the art, these steps clearly distinguish over and are not obvious from the teachings of known prior art and in particular over Yoshihara '177 and Chung '650. Further, one skilled in the art would not look to the teachings of

Yoshihara '177 and Chung '650 to arrive at the claimed inventions as identifi4ed in Claims 2 and 11.

9. The method for manufacturing an array of hermetically sealed SAW devices as presented in the claims pending in this application have resulted in the commercial success of product delivered by Sawtek, Inc. to its customers. For example, the array process of flip-chip devices as taught in this patent application of Chuck Carpenter has been successfully applied to the high volume production for a number of SAW filters for application in mobile telecommunication systems. At least a million of such devices have been produced in the last couple of years with a desirable assembly yield that reflects the "robustness" and value of the claimed process.

10. I hereby declare that all statements made herein of my own accord are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that any such willful false statements may jeopardize the validity of the application or any patent issued thereon.

9/23/04
Date

J. Chocola
Jack R. Chocola